D 70188 (Pages : 2) Name.....

Reg. No.....

FIFTH SEMESTER B.Sc. DEGREE EXAMINATION, NOVEMBER 2019

(CUCBCSS–UG)

B.C.A.

BCA 5B 08—COMPUTER ORGANISATION AND ARCHITECTURE

(2017 Admissions)

Time : Three Hours Maximum : 80 Marks

Part A

Answer **all** *questions.*
Each question carries 1 *mark.*

1. Which digital system translates coded characters into a more intelligble form ?
2. In a BCD to seven segment converter, what is the use of code converter ?
3. Which shift register that will accept a parallel input and can shift data left or right called ?
4. In this type of counter, the complement of the output of the last stage of the shift register is fed back to the D input of the first state.
5. How register reference instructions are recognized by the control unit ?
6. How do we implement the control logic in hardwired logic ?
7. ——— contains the status information that characterizes the state of the CPU.
8. Write the reverse polish notation for the given ainfils arithmetic expression A * B + C * D + E * F.
9. How many characters can be encoded using ASCII ?
10. ——— is the method transfers a large block of data between a high speed I/O device such as a disk and memory directly without CPU.

(10 × 1 = 10 marks)

Part B

Answer **all** *questions.*
Each question carries 2 *marks.*

11. Draw the logic diagram of a 2-line-to-4-line decoder using NOR gates.
12. Draw the logic diagram of a four-bit binary ripple countdown counter, using flip-flops that trigger on the negative edge of the clock.
13. What do you meant by instruction cycle ? What are the four phases of instruction cycle ?
14. Explain about the input output configuration with neat figure.
15. What do you mean by register stack ?
16. What do you mean by Data Transfer Instructions ?

Turn over

17. Define hit/miss ratio.
18. What do you mean by I/O controllers ?

(8 × 2 = 16 marks)

Part C

Answer any **six** *questions.*
Each question carries 4 *marks.*

19. Decsribe the operation of a multiplexer with necessary diagrams.
20. Construct a 16 × 1 multiplexer with two 8 × 1 and one 2 × 1 multiplexers. Use block diagrams.
21. Explain the working of decade counter.
22. Explain about the control unit with figure.
23. Write a note on register reference instructions.
24. Explain about the priority interrupt.
25. What do you mean by data manipulation instructions ?
26. Write a note on peripheral devices.
27. What do you mean by memory mapping ?

(6 × 4 = 24 marks)

Part D

Answer any **three** *questions.*
Each question carries 10 *marks.*

28. (a) Explain the working of decoders with diagram.
    (b) Draw the logic diagram of 2-to-4-line decoder using (i) NOR gates only ; (ii) NAND gates only. Include the enable input.
29. Write a note on Johnson counter.
30. Discuss about the design of accumulator logic.
31. Discuss about the processor organization.
32. Discuss about the memory organization.

(3 × 10 = 30 marks)